Single electron tunnelling transistor with tunable barriers using silicon nanowire MOSFET

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Single-electron tunnelling (SET) transistors[1] are now of great and wide interest as basic elements for future applications such as low-power nanoelectronics[2] and read-out electrometer for solid-state quantum computing[3]. Silicon SET devices[4] have great potential because such applications inevitably rely on integration capability and stable operation[5]. We report the operation of SET transistors with tunable barriers using silicon nanowire MOSFET structures; these structuers are now being intensively studied for next-generation CMOS. We demonstrate tuning the conductance of tunnel barriers by more than three orders of magnitude. By using this flexible control of the barriers, we can demonstrate various configurations of charge islands in a single device; we observed the systematic

evolution from a single island to double islands. Also, in spite of a number of efforts to fabricated silicon SET transistors, no work has achieved sufficient controllability in device parameters. We obtained excellent reproducibility in the gate capacitances: values on the order of 10aF, with the variation smaller than 1aF. This flexibility and controllability both demonstrates that the device is highly designable to build a variety of SET devices based on CMOS technology.

The motion of individual electrons in solid state devices is controllable by utilizing the Coulomb blockade (CB)[6] in small tunnel junctions; the tunnelling of an electron is inhibited due to the charging energy. In the past decades, single-electron tunnelling (SET) devices have been extensively studied for a wide range of application such as low-power LSI[2,4], ultrasensitive electrometers[7], and metrological standards[8,9]. While the conventional metal-based SET devices use fixed tunnel barriers made of metal oxide, the use of electrostatic potential barriers by gate electrodes has become possible in semiconductor devices, e.g. in GaAs-based SET devices[10]. These barriers are electrically tunable, giving us a chance to control the tunnel conductance over a wide range and thereby providing the degree of freedom to control CB and/or the configuration of charge islands in a more flexible way.

Among semiconductor devices, silicon(Si)-based devices have been investigated mostly in the context of LSI application because of their integration capability and stable operation. In spite of the attempts to fabricate high-temperature (above 4 K, up to room temperature) operating devices with various techniques[4], it is still hard to see sufficient controllability in device parameters such as capacitance and tunnel conductance. Remarkably, even in devices for use at cryogenic temperature lower than 4K, in which the requirement for precision in device size can be relaxed, no work has

ever shown such reproducibility. It is important to develop a standard way of fabricating devices reproducibly and find out the scaling rule, as is always sought in Si device technology.

We report here the operation of Si SET transistors with tunable barriers fabricated by standard Si MOS technology. Each transistor consists of a Si nanowire channel and three fine gates that cross over it. When a negative voltage is applied to the gate, the electrostatic barrier is formed in the Si nanowire channel; this is exactly the switch-off mechanism of a MOSFET. If we use the electrostatic barrier produced by each of the Si MOSFETs, each with a high on-off ratio, we can tune the tunnel conductance of the barrier in a wide range. In similar prior reports[11,12], no clear demonstration of reproducibility and controllability was given.

The category of such devices with tunable electrostatic potential, sometimes what we call a Si nanowire charge-coupled device (CCD)[13], is also of emerging importance in fundamental research areas. In the metrology research SET devices such as turnstiles [14] and pumps[15] are expected to realize standards of the electric current that will provide the opportunity to test the ”metrological quantum triangle”[16]. The problem in conventional metal-based SET pumps with fixed tunnel barriers is that the current was limited to a few pA due to the maximum frequency of a few tens of MHz. Our SET devices with dynamically varied barriers have shown turnstile operation up to 100MHz[17,18]. A CCD-type device may also be a key element for Si-based solid-state quantum computing[19] which requires the control of the motion of a single electron that interacts with nuclear spin. In a previous report[20], We have also found our devices showed small but periodic CB oscillations of SET transistors at 20 K by means of a special voltage-sweep method.

Figure 1 (a) shows the schematic top-view and the cross sectional view of the device. The <110>-oriented Si-wire channel and lower poly-Si gates (LGS, LGC, LGD)

are fabricated by electron beam lithography on a (001) silicon-on-insulator wafer. The wide upper poly-Si gate (UG) is used as an implantation mask during the formation of n-type source and drain. The thicknesses of the Si wire, the gate SiO_2 and the buried SiO_2 are about 20, 30 and 400 nm, respectively. The length of the lower gates is 10nm. The UG intrudes into the 40nm-long gap between lower gates. The thickness of the spacer SiO_2 between lower gates and UG is 30nm. Figure 1(b) shows a top-view scanning-electron-microscope image of the device before the UG formation. The equivalent circuit diagram is depicted in Figure 1(c). Three tunable barriers are controlled by the gate voltages to lower gates (V_{LGS}, V_{LGC}, V_{LGD}). The region sandwiched between the barriers acts as a charge island, which is mainly controlled by the upper gate voltage (V_{UG}), but also is coupled to lower gates via cross capacitances. Tunable barriers allow us to get various configurations of the charge islands; for example, a long island is formed if two barriers are formed under LGS and LGD while a short island is formed if LGC and LGD form barriers.

Conductance (G) characteristics of a single barrier formed under LGD are shown in Fig. 2(a). The source was grounded while the drain voltage (V_D) was 1mV. V_{UG}, V_{LGS}, and V_{LGC} were fixed at 2V, 0V, and 0V. In the subthreshold region when $V_{LGD} < -1.9$ V, the conductance showed exponential dependence on V_{LGD}, which seems to resemble thermally activated conduction of the conventional MOSFET. However, because the slope was almost independent of temperature up to 10 K, we attribute the dominant conduction below 10 K to the source-to-drain tunnelling, as was reported previously using a 8nm-gate MOSFET[21]. It was possible to vary the tunnel conductance by more than three orders of magnitude down to the noise floor of our measurement.

We now describe the operation of SET transistors using the electrostatic barrier. Figure 2(b) shows G (V_{LGC}) characteristics of a SET transistor when two barriers are formed under LGS and LGD. V_{LGD} and V_{LGD} are set so that G of each barrier is equal to

1μS when V_{LGC} =0V. We obtained a highly periodic CB oscillation in a broad range of V_{LGC}, except for the region below V_{LGC}=-1 V where application of V_{LGC} forms a third barrier under LGC to split a long island into two islands. In the periodic region where V_{LGC}>-1 V the deviation of the oscillation period was less than one percent[22]. The inset of Fig.2b shows the G (V_{LGC}) curves for various conductances of the barrier. We were able to vary the peak conductance electrically by more than three orders of magnitude. We mention here that the CB was smeared out in a higher-conductance region. We believe that this behaviour is related to the interesting subject of how the CB is formed and lifted when the potential barrier is significantly low. Details of this subject will be reported separately.

We used the different configurations of charge islands to estimate various gate capacitances (C_G). C_G was calculated by e/ΔV where ΔV is the period of the CB oscillation. For example, Fig. 2 (c) shows the CB oscillations of the long island when UG was scanned, while Fig.2 (d) shows that of the short island formed between LGC and LGD. We can see that the upper gate capacitance (C_{UG}) of the short island was close to half that of the long island. A summary of the gate capacitances for three devices with an identical lithography design is in Table 1. It is remarkable that the variation in C_{UG} (22aF for the long island and 11aF for the short one) was quite small, about 1aF (about 10 % of 11aF) at most. The capacitances between the lower gates and islands (C_{LGS}, C_{LGC}, C_{LGD}) have also a variation smaller than 1aF, although the relative variation gets larger.

The measured capacitances agree fairly well with calculated ones using a simplified geometry model. The capacitance of a cylindrical Si wire with a skin of SiO_2 is given by $C_G = 2\pi\varepsilon L / \ln[(D_{OX} + D_{SI}/2)/(D_{SI}/2)]$; ε is the permittivity of SiO_2, L is the wire length, D_{OX} is the SiO_2 thickness, and D_{SI} is the wire diameter. For the short island, if we assume that UG is coupled to the wire part whose boundaries extend halfway

under the spacer SiO_2 on both sides, the corresponding L is 70nm. Then, C_{UG} 11.0aF when ε=3.9ε_0, D_{OX}=30nm, and D_{SI}=20nm. Similarly, for the longer island, C_{UG} and C_{LGC} are calculated to be 21.9 aF and 6.3 aF, respectively.

Figure 3 shows Coulomb diamond characteristics in the contour plot of the drain current vs V_{LGC} and V_D. The configuration was such that a long island was formed with tunnel barriers of conductance G=100 nS. From the shape of the diamond, we estimate the source and the drain capacitance to be about 6 aF for each. The total capacitance of the long island is therefore estimated to be 47 aF. The total capacitance of the short island with similar barriers is estimated to be about 30 aF.

Splitting of the charge island is demonstrated in Fig. 4. Figure 4(a) shows the equivalent circuit diagram. Figures 4(b)-(e) show the contour plots of the drain current vs V_{LGS} and V_{LGD}. We changed V_{LGC} as a parameter to split a long island into double short islands. In Figure 4(b) the central barrier is so low that the island is single; straight ridge lines corresponding to the peaks of CB oscillations run in parallel. As the barrier is raised in Fig. 4(c) and 4(d), the ridge lines are deformed into the so called honeycomb lattice[16] because the island is split into two coupled islands. In this transition where the coupling is tunable[23] a larger current is obtained at the vertices of the lattice. The two islands become more isolated in Fig. 4(e) where the lattice is deformed into the parallelogram one. Large currents are obtained only at the vertices where the CBs at the two islands are lifted at the same time. The systematic evolution from the single island to double islands demonstrates that the control of the electrostatic barrier is effective in making and changing various configurations of charge islands.

We believe that the excellent controllability in these devices increases the potential of Si-based SET devices for a wider range of application because the device parameters are designable, reproducible, and tunable. Moreover, we are hopeful that we

will be able to reduce the device size based on the scaling rule of MOSFETs; the devices presented here used the technology node between 45 nm and 65nm that should be commercially available soon, around 2008[24]. We can expect that higher temperature operation will be achieved by the progressing CMOS technology that will enter sub-10nm minimum feature size.

In conclusion, we demonstrated the operation of SET transistors with electrostatic barriers using Si nanowire MOSFETs. Tunnel barriers were tunable in their conductance over three orders of magnitude, which enabled us to change the island configuration flexibly and observe systematic evolution form a single island to split double islands. The charge-island gate capacitances on the order of 10 aF showed excellent reproducibility with the deviation less than 1aF.

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22. The electron number in the long island is estimated to be about 200 at VLGC =0V for the result in Fig.2b, which might be the reason why the island was highly metallic with periodic CB oscillations.

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Figure 1 The SET transistor using Si nanowire MOSFETS. a, Schematic top view and cross sectional view. Three lower gates (LGS, LGC, LGD) are used to form tunnel barriers. b, Top-view scanning-electron-microscope image of the device before the upper gate is formed. c, Equivalent circuit of the device with tunnel barriers separately tuned by V_{LGS}, V_{LGC}, and V_{LGD}.

Figure 2 Electrical characteristics (device 1). a, Conductance of a MOSFET at LGD as a function of V_{LGD} at V_D=1 mV (the characteristics of the single barrier). b, CB oscillation of the SET transistor consisting of the long island with two barriers (G=1μS) at LGS and LGD (T=1.5 K, V_{LGS}=-2.352 V, V_{LGD}=-1.902 V, V_D=1 mV, and V_{UG}=2 V). The inset shows the results when G of each barrier is 8 μS, 4 μS, 1 μS, and 20 nS. c, CB oscillation of the long island as a function of the upper gate voltage at V_{LGS} =-2.465 V, V_{LGC}=0 V, and V_{LGD}=-1.95 V. d, CB oscillation of the short island with tunnel barriers at LGC and LGD (V_{LGS}=0 V, V_{LGC}=-1.426 V, and V_{LGD}=-1.95 V). The configurations of tunnel barriers are schematically shown in each figure.

Figure 3 The Coulomb diamonds in the contour plot of the drain current vs V_D and V_{LGC} (device 1, T=0.02 K, V_{UG} =2 V, V_{LGS} =-2.483 V, V_{LGD} =-1.957V). Contour lines are 20 pA steps from low (red) to high (violet) in the range between - 460 pA and 390 pA.

Figure 4 Evolution from a single island to split double islands for the device 2. a, Equivalent circuit. b-e, Contour plots of the drain current vs V_{LGS} and V_{LGD} (T=0.02 K, V_D=1mV, V_{UG}=2V, V_{LGC}=-0.75 V, -1.13 V, -1.18 V, and -1.284 V, respectively). Each V_{LGC} is depicted by the arrow in Figure 2 b. Contour lines run from low (red, 0 A) to high (violet, 1.4 nA) with 10pA steps.

Table 1 Gate capacitances in three devices with the same designed pattern sizes

Capacitances to charge island	device1	device2	device3
Long island			
C_{UG}	22 aF	22 aF	22 aF
C_{LGS}	3.2 aF	2.7 aF	3.0 aF
C_{LGC}	6.7 aF	6.2 aF	6.0 aF
C_{LGD}	2.5 aF	2.5 aF	2.8 aF
Short island (source side)			
C_{UG}	10 aF	11 aF	10 aF
C_{LGS}	2.8 aF	2.3 aF	2.9 aF
C_{LGC}	***** [1)]	2.8 aF	2.6 aF
C_{LGD}	0.08 aF	0.14 aF	0.08 aF
Short island (drain side)			
C_{UG}	11 aF	11 aF	11 aF
C_{LGS}	0.09 aF	0.12 aF	0.07 aF
C_{LGC}	***** [1)]	3.1 aF	2.8 aF
C_{LGD}	2.4 aF	2.4 aF	2.5 aF

Table 1 shows the capacitances estimated from the CB oscillations for three identically patterned devices. The three possible configurations forming a single charge island are described: a long island (barriers formed by LGS and LGD), a short island (two barriers by LGS and LGC), and a short island island (two barriers by LGC and LGD). [1)] Not measured.

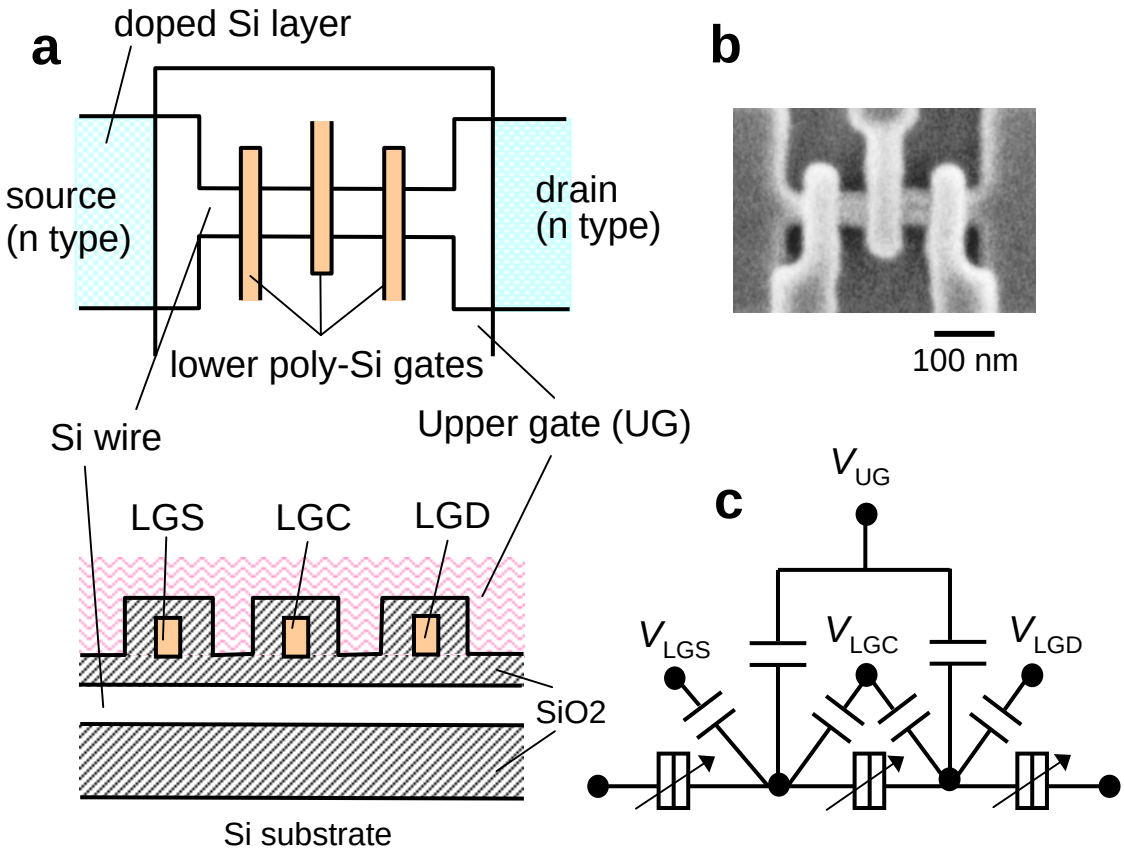
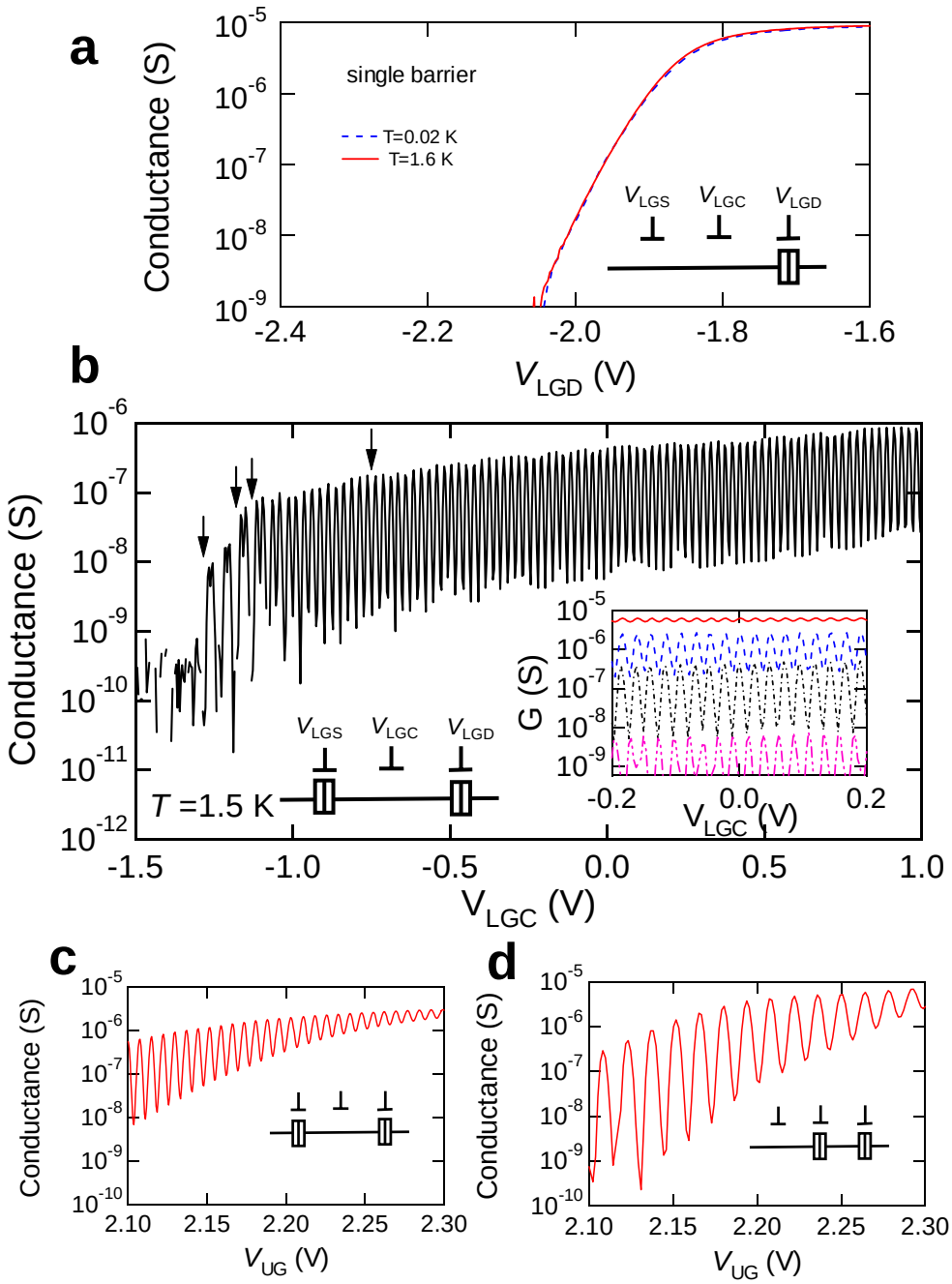


Fig. 1 Fujiwara et al.



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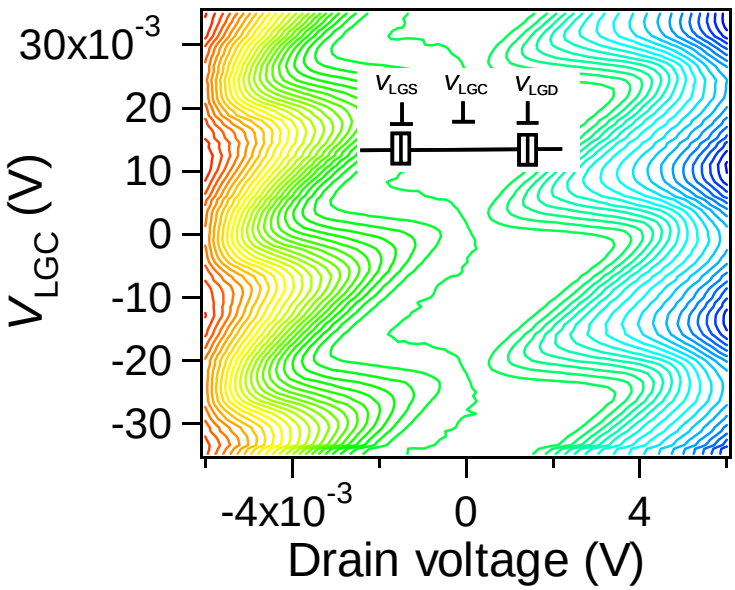

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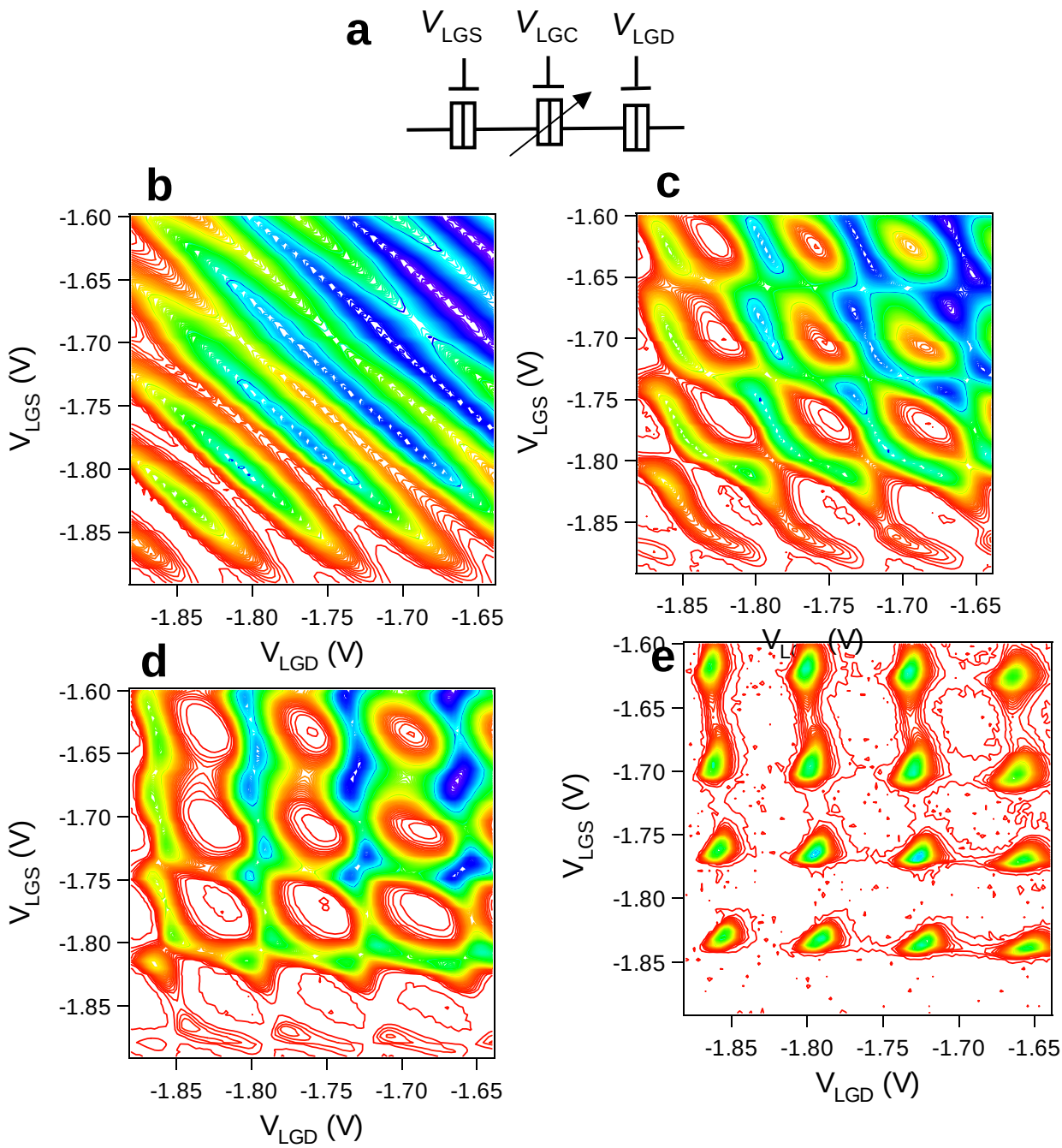

Fig. 4 Fujiwara et al.